RECEIVED
CENTRAL FAX CENTER
DEC 1 1 2007

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-17. (canceled).

18. (withdrawn): A method for forming a thin film transistor liquid crystal display (TFT-LCD), the TFT-LCD having at least one thin film transistor (TFT) and one storage capacitor (Cs), the method comprising the steps of:

providing a substrate;

depositing a first conductive layer and a second conductive layer above the substrate to form a gate electrode of the TFT and a bottom electrode of the storage capacitor;

forming an insulating layer on the first and second-conductive layers and the substrate;

depositing a semiconductor layer and a doped silicon layer on the insulating layer;

forming a sacrifice layer with an island shape on the doped silicon layer, and the sacrifice layer being positioned directly above the first conductive layer;

forming a metal layer covering the sacrifice layer and the doped silicon layer;

patterning the metal layer to form a source electrode and a drain electrode above the first conductive layer as well as to form a shielding metal layer above the second conductive layer, a channel being defined between the source electrode and the drain electrode to expose the sacrifice layer in the channel, a capacitor region being defined as a portion of the substrate covered by the shielding metal layer, and a non-TFT region being defined as a portion of the substrate not covered by the source electrode, the drain

electrode, the capacitor region, and the channel so as to exposed the doped silicon layer thereon;

using the source electrode, the drain electrode, and the shielding metal layer as a mask to perform the following etching processes at the same time: (a) removing the doped silicon layer and the island-shaped sacrifice layer in the channel so as to expose the semiconductor layer therein, and (b) removing the doped silicon layer and the semiconductor layer in the non-TFT region so as to expose the insulating layer thereon; and

forming a passivation layer to cover the source electrode, the drain electrode, the channel, and the capacitor region.

19. (withdrawn): The method of claim 18, wherein during the etching process, etching rates of the island-shaped sacrifice layer, the doped silicon layer, and the semiconductor layer are RIS, Rn, and Ra respectively, the thickness of the island-shaped sacrifice layer, the doped silicon layer, and the semiconductor layer are TIS, Tn, and Ta, and the time for removing the island-shaped sacrifice layer and the doped silicon layer in the channel (TIS/RIS+Tn/Rn) is not less than the time for removing the doped silicon layer and the semiconductor layer in the non-TFT region (Tn/Rn+Ta/Ra).

20. (withdrawn): The method of claim 18 further comprising the following steps: patterning the passivation layer to form a first hole and a second hole so as to expose one of the source electrode and the drain electrode through the first hole, and expose the shielding metal layer in the capacitor region through the second hole; and

forming a transparent conductive layer above the passivation layer, the transparent conductive layer being electrically connected to one of the source and the drain electrodes through the first hole, as well as electrically connected to the shielding metal layer through the second hole for forming an upper electrode of the storage capacitor.

21.-25. (canceled)

26. (withdrawn): A method for manufacturing a thin film transistor liquid crystal display (TFT-LCD), the TFT-LCD having at least one thin film transistor (TFT) and one storage capacitor, the method comprising the steps of:

providing a substrate;

depositing first and second conductive layers above the substrate to respectively form a gate electrode of the TFT and a bottom electrode of the storage capacitor;

forming an insulating layer above the first and second conductive layers and the substrate;

forming a semiconductor layer on the insulating layer;

forming a sacrifice layer with an island shape on the semiconductor layer, and the sacrifice layer being positioned directly above the first conductive layer;

depositing a doped silicon layer to cover the sacrifice layer and the semiconductor layer;

forming a metal layer covering the doped silicon layer;

patterning the metal layer to form a source electrode and a drain electrode above the first conductive layer, as well as to form a shielding metal layer above the second conductive layer;

a channel being defined between the source electrode and the drain electrode to expose the doped silicon layer therein;

a capacitor region being defined as a portion of the substrate covered by the shielding metal layer; and

a non-TFT region being defined as the substrate not covered by the source electrode, the drain electrode, the capacitor, and the channel so as to expose the doped silicon layer thereon;

using the source and drain electrodes and the shielding metal layer as a mask to perform these etching processes at the same time: (a) removing the doped silicon layer

and the island-shaped sacrifice layer in the channel so as to expose the semiconductor layer in the channel, and (b) removing the doped silicon and semiconductor layers in the non-TFT region to expose the insulating layer therein; and

forming a passivation layer to cover the source electrode, the drain electrode, the channel, and the capacitor region.

27. (withdrawn): The method of claim 26, wherein during the etching process, etching rates of the island-shaped sacrifice layer, the doped silicon layer, and the semiconductor layer are RIS, Rn, and Ra respectively; the thickness of the island-shaped sacrifice layer, the doped silicon layer, and the semiconductor layer are TIS, Tn, and Ta; and the time for removing the doped silicon layer and the island-shaped sacrifice layer in the channel (TIS/RIS+Tn/Rn) is not less than the time for removing the doped silicon layer and the semiconductor layer in the non-TFT region (Tn/Rn+Ta/Ra).

28. (withdrawn): The method of claim 27 further comprising the following steps:

forming a first hole and a second hole in the passivation layer so as to expose one of the source and drain electrodes via the first hole, and expose the shielding metal layer via the second hole; and

forming a transparent conductive layer above the passivation layer, the transparent conductive layer being electrically connected to one of the source electrode and the drain electrode through the first hole, as well as electrically connected to the shielding metal through the second hole for forming an upper electrode of the storage capacitor.

29. (currently amended) A thin film transistor (TFT), comprising:

a gate electrode with an island shape formed on a substrate;

an insulating layer covering the gate electrode;

a semiconductor layer with an island shape formed on the insulating layer, and

positioned directly above the gate electrode;

a source doped silicon layer and a drain doped silicon layer formed on the semiconductor layer, a channel being defined between the source doped silicon layer and the drain doped silicon layer to expose the semiconductor layer therein;

first and second sacrifice layers with island shapes respectively formed on the source doped silicon layer and drain doped silicon layer and formed over the semiconductor layer, the first and the second sacrifice layers being spaced apart by the channel and further separate from the insulating layer in their entirety, wherein an entire bottom of the first and second sacrifice layers is higher than an top of the semiconductor layer;

a source electrode formed above the first sacrifice layer and the source doped silicon layer; and

a drain electrode formed above the second sacrifice layer and the drain doped silicon layer,

wherein the first sacrifice layer is only formed on a portion of a doped silicon layer chosen between the source doped silicon layer and the drain doped silicon layer, and the respective source or drain electrode directly contacts a portion of the doped silicon layer not covered by the respective first sacrifice layer or second sacrifice layer.

30. (withdrawn): The method of claim 37, wherein an etching rate of the first and the second sacrifice layers is R_{IS}, an etching rate and a thickness of the drain doped silicon and the source doped silicon layers are R_n and T_n, and an etching rate and a thickness of the semiconductor layer are R_a and T_a, and the thickness of the first and the second sacrifice layers T_{IS} meets an equation of $(T_{IS}/R_{IS}+T_n/R_n) \geq (T_n/R_n+T_a/R_a)$.

31. (original) The TFT in claim 29, further comprising a passivation layer covering the source electrode, the drain electrode, and the channel, and the TFT is used in an in-plane-switch (IPS) type LCD.

32. (original) The TFT in claim 29, further comprising:

a passivation layer covering the TFT on the substrate, and having a hole above the drain electrode; and

a transparent conductive layer formed above the drain electrode and electrically connected to the drain electrode via the hole.

33. (currently amended) A thin film transistor (TFT), comprising:

a gate electrode with an island shape formed on a substrate;

an insulating layer covering the gate electrode;

a semiconductor layer with an island shape formed on the insulating layer, and positioned above the gate electrode;

first and second sacrifice layers with island shapes formed over and in direct contact with the semiconductor layer in their entirety, and a channel being defined between the first and second sacrifice layers so as to expose the semiconductor layer;

a source doped silicon layer and a drain doped silicon layer formed above the first sacrifice layer, second sacrifice layer, and the semiconductor layer, the source doped silicon layer and the drain doped silicon layer being spaced apart by the channel~~, wherein the source doped silicon layer and the drain doped silicon layer contact with the semiconductor layer~~; and

a source electrode and a drain electrode respectively formed on the source doped silicon layer and the drain doped silicon layer,

wherein the first sacrifice layer is only disposed below a portion of a doped silicon layer chosen between the source doped silicon layer and the drain doped silicon layer, and the respective source doped silicon layer or drain doped silicon layer directly contacts a portion of the semiconductor layer.

34. (withdrawn): The method of claim 38, wherein an etching rate of the first and the

second island-shaped sacrifice layers is R_{IS}, an etching rate and a thickness of the drain doped silicon and the source doped silicon layers are R_n and T_n, an etching rate and a thickness of the semiconductor layer are R_a and T_a, and the thickness of the first and the second sacrifice layers T_{IS} meets an equation of $(T_{IS}/R_{IS}+T_n/R_n) \geq (T_n/R_n+T_a/R_a)$.

35. (original) The TFT in claim 33, further comprising a passivation layer covering the source electrode, the drain electrode, and the channel, and the TFT is used in an in-plane-switch (IPS) type LCD.

36. (original) The TFT in claim 33 further comprising:

a passivation layer covering the TFT on the substrate, and having a hole above the drain electrode; and

a transparent conductive layer formed above the drain electrode and electrically connected to the drain electrode via the hole.

37. (withdrawn): A method comprising:

forming the TFT claimed in claim 29;

wherein forming the TFT includes

etching the source doped silicon layer;

etching the drain doped silicon layer;

etching the first and second sacrifice layers for a first selected period of time and;

etching the semiconductor layer for a second selected period of time substantially equal to the first selected period of time.

38. (withdrawn): A method comprising:

forming the TFT claimed in claim 29;

PAGE 8/15 * RCVD AT 12/11/2007 8:00:05 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/9 * DNIS:2738300 * CSID:323 934 4145 * DURATION (mm-ss):03-52

wherein forming the TFT includes

etching the source doped silicon layer;

etching the drain doped silicon layer;

etching the first and second sacrifice layers for a first selected period of time and;

etching the semiconductor layer for a second selected period of time substantially equal to the first selected period of time.

* * * * *